

10/080568

LAW OFFICES OF
McGINN & GIBB, PLLC

A PROFESSIONAL LIMITED LIABILITY COMPANY
PATENTS, TRADEMARKS, COPYRIGHTS, AND INTELLECTUAL PROPERTY LAW
8321 OLD COURTHOUSE ROAD, SUITE 200
VIENNA, VIRGINIA 22182-3817
TELEPHONE: (703) 761-4100
FACSIMILE/DATA: (703) 761-2375; 761-2376
E-MAIL: MCGINNGIBB @ AOL.COM

SEAN M. MCGINN
PHILLIP E. MILLER†
FREDERICK E. COOPERRIDER†
PETER A. BALNAVE, PH.D.
FREDRIC J. ZIMMERMANT
JAMES E. HOWARD†
KENDAL M. SHEETS
CHRISTOPHER M. MCGINN*
*MEMBER OF BAR OTHER THAN VA
*PATENT ENGINEER (NONATTORNEY)

ANNAPOLIS, MD OFFICE
FREDERICK W. GIBB, III
MOHAMMAD S. RAHMANT
LAWRENCE A. SCOTT†

FAX RECEIVED

MAY 27 2003

TECHNOLOGY CENTER 2800

May 27, 2003

VIA FACSIMILE

To: Examiner Phat X. Cao
Group Art Unit No. 2814
U.S.P.T.O.

Facsimile No.: (703) 872-9319

From: Phillip E. Miller

Facsimile No.: (703) 761-2375 or 76

Re: Enclosed § 1.116 Amendment
U.S. Patent Application Serial No. 10/080,568
Our Reference: YOR.324DIV

Dear Examiner Cao:

Enclosed is the Amendment, responsive to the March 27, 2003 Office Action, which should place the above-referenced case in condition for allowance.

Thank you in advance for your consideration on this case.

Very truly yours,



Phillip E. Miller

PEM/tw
Enclosure

Total No. of Pages Transmitted: 17

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Stephen M. Gates, et al.

Serial No.: 10/080,568

Group Art Unit: 2814

Filed: February 25, 2002

Examiner: Phat X. Cao

For: FORMATION OF ARRAYS OF MICROELECTRONICS ELEMENTS

Honorable Commissioner of Patents
Alexandria, VA 22313-1450
BOX AF

FAX RECEIVED

MAY 27 2003

TECHNOLOGY CENTER 2800

AMENDMENT UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action dated March 27, 2003, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims to read as follows:

11. (Amended) An array of microelectronic elements comprising:
- a substrate of semiconductor material;
 - a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto;
 - a pattern of mutually electrically isolated conducting regions disposed within said lower layer of dielectric material, said conducting regions extending to said upper surface of said lower layer;
 - an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer; and
 - a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer,
- wherein each conducting region comprises:

PLEASE
DO NOT ENTER
PC
6/2/03

#7C Aut
J/E M. Brunson
5/29/03